WHAT IS CLAIMED IS:

1. A programming method for multilevel non-volatile memory cells comprising a first step wherein predetermined bias voltages are applied to the cell gate, drain and source terminals and providing a following control step of the programming just occurred by means of a programming algorithm of the program-verify type, wherein the control step is skipped for some cells which have to reach a predetermined logic state.

2. A method according to claim 1 wherein said predetermined logic state is the state "00".

3. A method according to claim 1 wherein the control of said some cells is performed only after a part of the remaining cells has reached the programmed state.

4. A method according to claim 1 wherein the control step for said some cells is skipped by connecting to a ground potential reference the bit-line whereto these cells are connected.

5. A method according to claim 4 wherein it provides the use of a logic disabling network associated with the control circuit portions of the memory device.

6. A multilevel non-volatile memory electronic device integrated on a semiconductor and comprising a matrix of non volatile memory cells, each cell being equipped with at least a floating gate transistor with gate, drain and source terminals, and comprising programming and control circuit portions associated with the cell matrix, wherein the control circuit portion comprises a logic network to disable the reading step only for some cells having to reach a predetermined logic state.

7. A device according to claim 6 wherein said predetermined logic state is the state "00".

8. A device according to claim 6 wherein the control of said some cells is enabled only after a part of the remaining cells has reached the programmed state.

9. A device according to claim 6 wherein the control of said some cells is disabled by connecting to a ground potential reference the bit-line whereto these cells are connected.